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LaurTec

EMC Testing

PCB Layout
Understand stray capacitance and inductance

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PCBWay

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Abstract

The PCB board layout is the last challenge after having designed the schematic. While things may work on sub-modules level, once all the system gets assembled on the PCB, additional problems may occur. Several "Tips and Tricks Cookbooks" are providing recommendations to the designer making the PCB layout the right way. Nevertheless properly understanding the limitation and boundary conditions at which a certain rule can be used, is fundamental. Thus, in this article, rather than talking about "Tips and Tricks" we will go down to the details of understanding from where the stray capacitance and inductance come from. Indeed, the two are responsible of the major problems a wrong layout may cause at system level.

Which path will the current take?

If we compare the current flow to a person, we will not be surprised to see that to go from point A to point B, both will take the easiest path. The "easy path" has an energy interpretation and can be rephrased saying that both will take the path that requires less energy. This is equivalent to the statement that says: "The current will flow through the path with less impedance". A generic impedance can be seen made of two components, the real part R and the reactance part X. Each PCB trace will have a certain impedance.

$$Z = R + iX$$

The contribution on the first part, comes from what we call Resistor. The second Ohm's law describes how the resistance depends on the trace width, height, the length and the material electrical properties. The width and length can be directly controlled during the layout phase, while the trace height, or thickness, is a PCB manufacturing propriety that can be requested to the PCB Manufacturer. This is provided in copper per square meter or directly in μm, 1 oz copper is equivalent to 35μm.
The trace reactance, comes from the stray capacitance (C) and inductance (L). Typically both C and L are not desired, thus the designer needs to make sure to keep them under control. L represents the component that models the amount of magnetic energy that gets stored in a certain volume, while C is the complementary component that depicts the amount of electric field energy that gets stored in a certain volume. From another perspective the ability to store energy, also means that the PCB path that contains the high C and L may create energy steps that may lead the current to flow through another path with less energy requirements (less impedance). Nevertheless whatever an impedance may be, the current must take a path to ground, thus, if only the high impedance path is available, the current will take that one.

What are C and L?

There are different definitions for C and L, depending on which aspect must be highlighted. Typically the most used are the ones below.

The C definition is:

$$C=\frac{Q}{V}$$

Which states that C is equal to the ratio of the charge Q and the voltage across the accumulated charges. For a standard capacitor with parallel plates, Q would be the accumulated charge on the plates, while V would be the voltage across the plates.

L definition is:

$$V(t)=-\boldsymbol{L}\frac{di(t)}{dt}$$

The definition derives from the Faraday Neumann Lenz law, and states that the voltage drop on the inductor, is proportional to L and the variation rate of $i(t)$ (I' m just ignoring the -).
If we want to determine the Capacitance or the Inductance we have on a certain PCB trace, we may use formulas from RF Handbooks. The equations we can find on those books apply on specific types of traces, such as Microstrips, which must be properly designed to make sure that the mathematical model to predict C and L would work out. Those formulas allow to determine the trace characteristic impedance out of the mechanical size, layer on which the trace is located, distance from ground and the PCB dielectric constant.
RF traces typically requires a lot of PCB area, which can be justified if you are designing an RF system and you need a controlled impedance trace. Typically on standard PCBs, the traces are much closer to each other, they cross other traces and they may have ground layers close by. That complexity does not really let the designer determine the actual stray C and L just out of formulas. Thus it is more important to understand how to limit stray C and L rather than determining an absolute value (unless you are designing an RF system).
While the Handbook's formulas may not apply to PCB with complex routing, the first two formulas of C and L we have just introduced as their definitions, do not help either. The definitions are correct, but we need to rephrase it from E and B fields perspective. Once we see C and L from the E and B fields, we can better understand what the stray C and L are and how we can limit it, if we need to.
For the C definition, we do not need to change that much to get the E field perspective. We must just recall that the Voltage V is defined as the linear integral of the electric field E, thus the C definition can be rewritten mostly the same way, just by changing V(t) with:

$$V(t)=\int_{x_1}^{x_2} E\,\boldsymbol{d}\,s$$

For L, things are different, indeed we need to define it from a different perspective. L can be defined in this way as well:

$$\boldsymbol{\Phi}(B)=\boldsymbol{L}\cdot i(t)$$

This states that the B flux $\boldsymbol{\Phi}(B)$ that gets concatenated within the area made by the electrical loop where $i(t)$ flows, is proportional to L. So, if have a current $i(t)$ that flows within a wire, that make a loop of area S, the magnetic field B that gets concatenated with S (either generated or not by $i(t)$), is proportional to L. The bigger is the loop the bigger would be L. If we make more loops, as typically an inductor is made of, each loop concatenates the magnetic field B, thus the total L increases.
Now we have both definitions of C and L from the E and B fields perspective. Recalling how the vectors sum up, we can intuitively sum in the space the B and E fields generated by a current $i(t)$. Depending on the direction the current is flowing (+ the current enters the page, while – is getting out the page), we have a different distribution of the charges, thus both the E and B fields may be different *out t of the same layout*. An example is shown in Figure 1 which depicts a simple PCB section with two traces (the field lines are simplified).

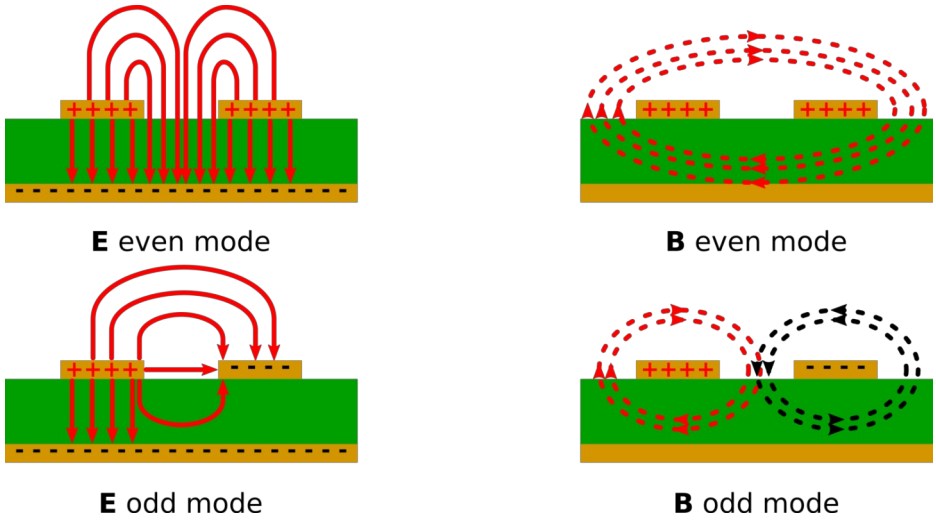

Figure 1: *PCB sections with two traces depicting the Even Mode and Odd Mode.*

Two scenarios are considered from the E and B fields perspective. The case where the currents flow in the same directions (Even Mode) and the case where the currents flow in opposite direction (Odd Mode). The Even Mode represents the typical use case where there is a data bus, where multiple lines travel in parallel on the PCB and the return path for the current is the ground layer. The Odd Mode represents the scenario where the signal trace

has a return path next to it, via an additional trace.
From Figure 1, out of the E and B fields lines distribution, it is possible to see that out of the same PCB layout, depending on the current flow, the field distribution density, thus the E and B fields intensity, are different. Considering how we have defined C and L, as the components that respectively store Electric and Magnetic field energy, it is possible to see that stray C and L would be different depending on current flow directions. Furthermore, different C and L could be defined, depending on the area we are considering. For instance we have a trace to ground capacitance (one per trace) and trace to trace capacitance.

PCB layout example

Reducing stray C and L with proper layout, it means that within our PCB and also from radiated Electromagnetic field perspective, we can reduce unwanted noise, which helps passing EMI tests such as the ones defined within the CISPR standards. The simple test setup shown in Figure 2, was used to indirectly measure, via a magnetic probe, the B field generated by a PCB trace terminated with a 50ohm. The circuit was fed via the spectrum analyzer tracking generator at 0dBm with a frequency between 1MHz-1GHz. The magnetic probe was directly connected to the spectrum analyzer input channel and placed 13mm above the PCB. A simple 3D printed PLA fixture was used to keep the setup mechanically stable.

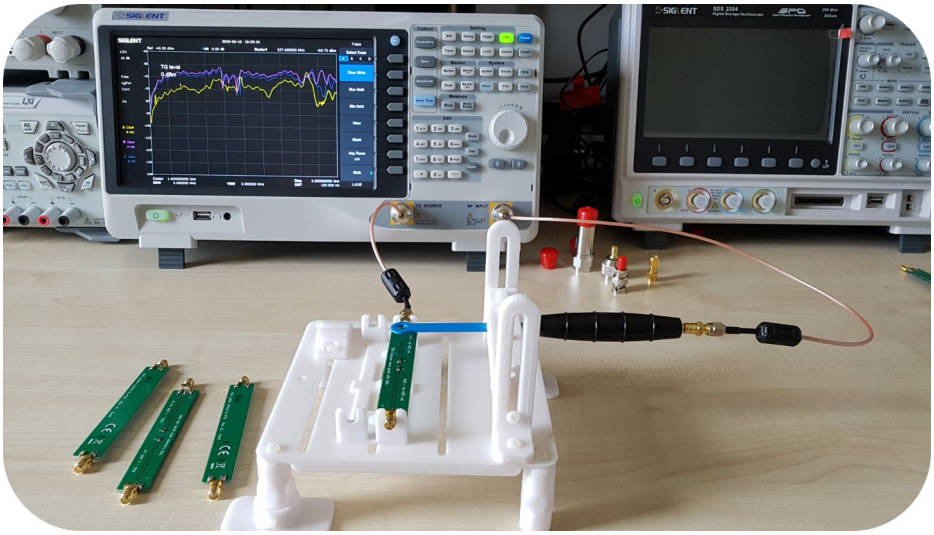

Figure 2: *PCB test setup.*

Different PCBs have been tested showing how a simple PCB trace could generate a B field and how B increases by increasing the current loop area. Figure 3 shows the different boards used on the test setup and the PCB transversal section. A real trace loop has been made on each board to easy the probe coupling. Tested diameters were 2.0mm Board 2, 2.5mm Board 3, 3mm Board 4. All the boards have been compared with a simple trace without any

horizontal trace loop. Each board has a straight trace on the bottom side for the current return path. For Board 1, this means that the return current mirrors the main trace (Odd Mode for B). The other boards with the trace loops, have two different layouts on the bottom side. One with a solid ground (left side) and one with a simple straight trace (right side). This means that the top trace with the loop does not have a mirrored current on the bottom side.

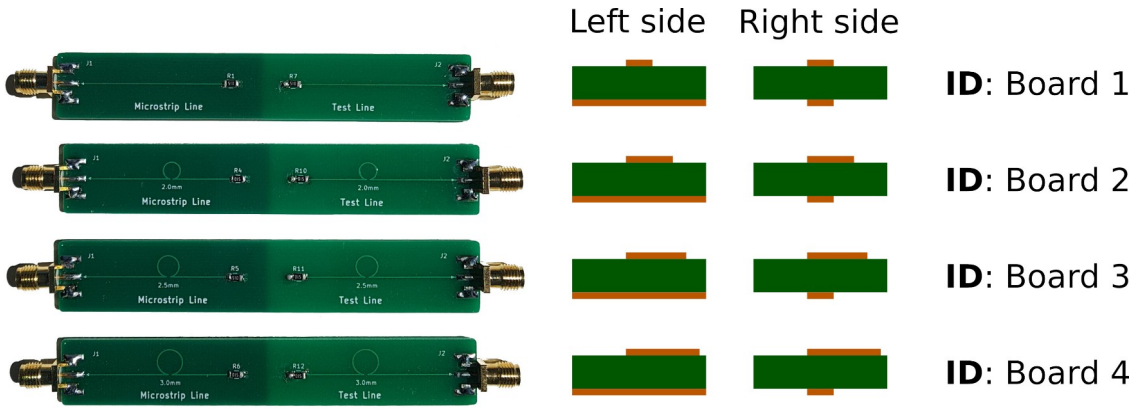

Figure 3: *PCB used for the tests with the transversal section details.*

Figure 4, shows the intensity of the B field coupled with the probe out of the Board 4.

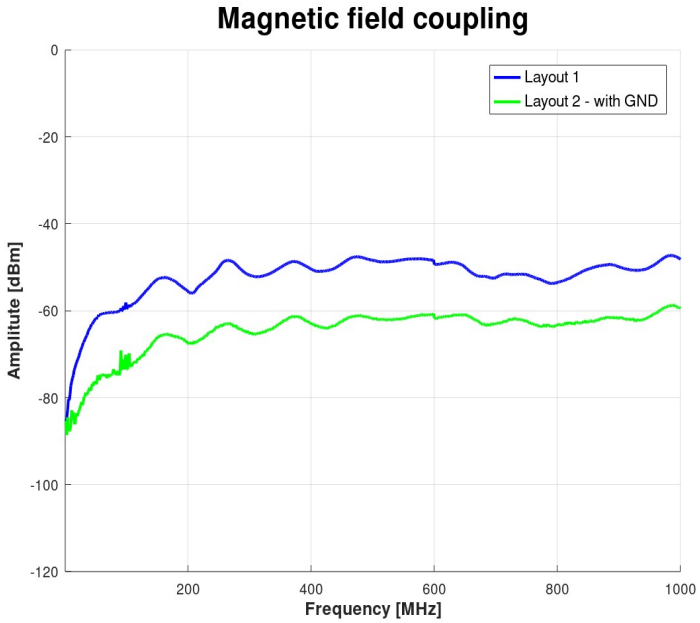

Figure 4: *B field energy coupled from the Board 4, by testing both left (green line) and right side (blue line).*

In particular the blue line is proportional to the B field generated by the layout without a ground layer (right side). The green line is the measure taken on the loop that has a solid ground underneath (left side).

The B field attenuation is related to the fact that for Layout 1, the current loop really creates an area as big as the loop made on the PCB (28.3mm^2) and this area is parallel to the magnetic probe. For the second layout, since there is a ground layer underneath, the current can flow just below the loop, thus the loop area is made from the distance between the traces and the circumference of the loop. By using 2 layers PCB the area would be 30.1mm^2 (1.6mm PCB thickness), while using 4 layers PCB, the area would be 2.1mm^2 if the GND layer is placed 0.11mm away from the top layer. Thus, using 4 layers PCB greatly reduces the stray L simply having a GND layer located on the second layer. On the other hand, Figure 4 has been taken with 2 layers PCB and still showed a reduction of the B field coupled with the probe. This is due to the fact that with the GND layer we are in the Odd Mode scenario and the B field cancel out once you move away from the traces, since the field lines rotate the opposite directions (Figure 1). Out of this considerations, knowing the stacking used by the PCB manufacturer is very important to determine the loop area benefit you can achieve by moving a trace from one layer to another. PCBWay offers this information directly online. For 4, 6 and 8 layers, the information can be found in the following link.

Figure 5, shows how by increasing the loop area, the magnetic field coupled energy increases. The coupled signal increases circa 15dBm by moving from 12.6mm^2 to 28.3mm^2 loop area.

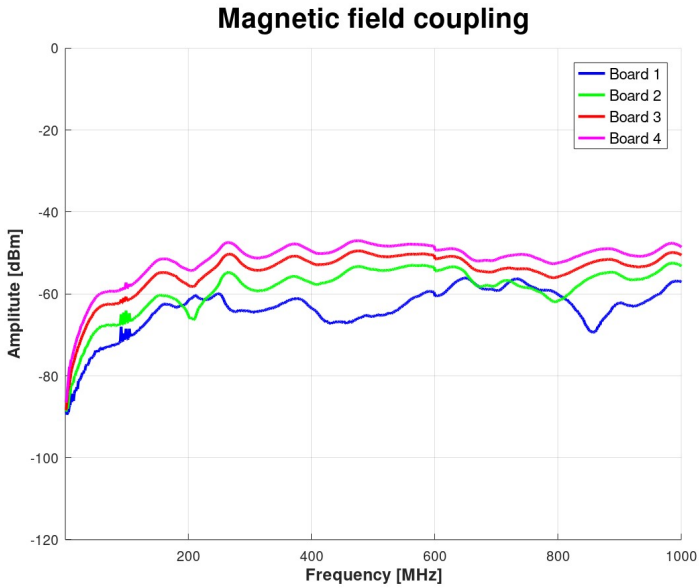

Figure 5: *B field energy coupled from the Boards 1-4, by testing the right side.*

Note
Around 88-108MHz, is possible to see the FM radio signals coupling with the setup.

Conclusions

In this article we have seen that the PCB traces can cause stray C and L depending on the current flow directions. This result has been deducted by defining the C and L from the E and B fields perspective. With that representation is possible to understand that the same PCB trace could act with different stray C and L, simply by changing the current flow by the next adjacent trace. Thinking from the E and B perspective, should help reduce stray C and L, designing a better PCB Layout.

About PCBWay

As one of the most experienced PCB manufacturers for prototyping and low-volume production in China, PCBWay is committed to meet the needs of customers from different industries in terms of quality, delivery, cost-effectiveness. With years of accumulated industry experience, PCBWay has customers from all over the world. The brand has became the first choice for the clients, thanks to its high strength and special services, such as:

- PCB prototyping and manufacturing FR-4 and Aluminum boards, but also advanced PCB like Rogers, HDI, Flexible and Rigid-Flex boards.
- PCB assembly.
- Layout and design service.

Bibliography

[1] www.LaurTec.it: official site where you can download the "EMC Testing" series.
[2] www.PCBWay.com: PCB manufacturer that sponsored the PCBs.
[3] PCBWay staking information (link).

History

Date	Version	Author	Revision	Description
08. Nov. 2020	1.0	Mauro Laurenti	Mauro Laurenti	Original version.