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EMC Testing

PCB ground layer considerations

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Abstract

Old system assemblies, based on vacuum tubes, were often made directly on the manufacturing floor without any PCB support. With the increased signal frequency and system integration, made possible by transistors and ICs, using a PCB was a must. Nevertheless, till the 80', regulations were not covering commercial products as they do today. EMC (Electromagnetic Compatibility) and immunity tests are today part of the system requirements that may challenge the designer during the design phase. High-speed applications, precision analog, and the regulations that the system must fulfill, make the PCB a fundamental part of the design puzzle. In this article, we will take a closer look at the PCB ground layer. Using it is very important, but sometimes it could lead to more problems than benefits...

Ground layer, pro and cons

Using a ground layer as part of the PCB layout is very important to reduce the radiated electromagnetic field. In particular, a solid ground layer should be used on the PCB. This is, in general, true but let's take a closer look at the "why" so that we can better understand where some tread-off might be needed. Having a solid ground layer means that it should not have slots that interrupt or open it. Indeed, having a slot may vanish some befits for which the ground layer is introduced. To guaranty a solid ground, in general, at least 4 layers may be needed, unless the schematic is relatively easy that can be routed on one layer, keeping the second layer as ground. If we have enough layers that allow us to keep one for Vcc as well, it will let the ground layer together with the Vcc layer, act as a distributed capacitor. A capacitor with metal parallel plates has a capacitance that is inversely proportional to the distance of the layers, thus having the GND and Vcc layer adjacent, helps to increase the capacitance. If there is a signal layer between GND and Vcc, the distance will increase, reducing the capacitance. While having both GND and Vcc layer is in general beneficial, because you have some energy stored within the PCB itself, the real benefit of having both the ground layer and Vcc layer is because of the layout itself. Indeed, the traces for the bypass capacitors and power supplies for each ICs can be easily routed, making it very short. Having a short trace translates to the stray inductance being reduced. The inductance has a voltage droop on its terminals as defined by the following equation:

$$V(t) = -\boldsymbol{L}\frac{di(t)}{dt}$$

Thus, it is opposite and proportional to the current variation rate. This means that if an IC will need quickly some energy, having a high stray L will create an energy delivery problem (delay). For this reason, the bypass capacitors of 0.1μF next to each IC helps, but making the stray L smaller will help further.

Reducing the length of the power supply traces can be achieved by having the GND and

Vcc layer. What can be done to reduce the traces inductance for those signal lines that necessarily have to go far from the ICs? In this case, the solid ground layer helps again, indeed each trace has some current and the current must flow to the ground. Having a ground layer next to a trace, allows the return current path to be just next to the trace. Reducing the loop area made of the trace and the return path on the GND layer, it reduces the stray L of the trace itself. Indeed, reducing the loop area means that less magnetic field can concatenate within the loop area. What has been just said, typically leads to the PCB stacking decision of having the GND layer just underneath the signal layer as shown in Figure 1 (solution A and B). Usually, the signal layer is on the top, while the GND layer is on the inner layer. This is done to limit the trace width vs. the current rate of the trace itself. Indeed, due to thermal consideration, a trace on the inner layer will increase the temperature T faster than a similar trace on the top layer. This would also increase the resistance together with the T increase. Thus, to allow a high current rate, a signal trace on the inner layer would need to be wider or ticker than a trace on the top layer with a similar current rate.

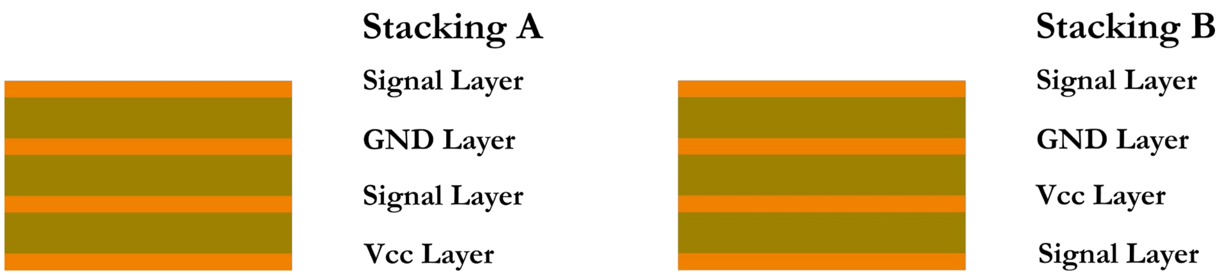

Figure 1: *PCB stacking examples.*

Sometimes the designer may also think of placing the signal traces within the PCB and put the GND on top of it as a shield. A metal sheet may indeed shield against an electromagnetic field. Nevertheless, if you try to shield an electromagnetic field you have to think twice, you need indeed to shield against an E field and a B field. The E field can be shielded by a copper layer since it has high conductivity and high εr. The copper μr is close to the air, thus it does not deviate the magnetic field B. Thus the GND layer can be used to shield if the traces are subject to high dV/dt and you try to limit the electric component that gets radiated. If the traces are more high current ones and with high di/dt, the ground layer will not properly shield the magnetic field. Furthermore, if you have high current traces, if you place those in the inner layer of the PCB, as mentioned, you may have thermal problems and you may be forced to use 70μm trace thickness rather than 35μm, trying to limit the trace impedance.

What has been said so far, should have already triggered an important takeaway, “the ground layer is good, but cannot always help”. There are cases where the GND layer can actually cause problems or reduce the system performances, thus we should understand the real benefits and eventually make some trade-off by removing or move the GND layer if not needed.

Ground layer, the bad things of it

In the following paragraph, we will describe some use cases where placing the GND layer needs some special thoughts. These cases should not be considered the only ones, but rather examples that should let the designer think twice before locating the GND layer as shown in Figure 1.

High speed Operational amplifiers

High speed means that the signal bandwidth (BW) of interest is high. This reflects the fact that the rate of voltage change is high, thus the harmonic content has high-frequency components. In the best case of a sinusoidal signal, dV/dt would be proportional to the amplitude of the signal and the signal frequency. From EMC perspective high BW means that you better try to reduce the stray inductance to limit the radiated field. While high dV/dt not necessarily means high di/dt, both would be proportional to the signal frequency. Thus, with high a BW signal, having a GND layer just underneath the signal trace is not a bad idea (Figure 1). Nevertheless, if we take a look at the PCB reference design of high-speed operational amplifiers, such as the OPA855 from Texas Instruments, we can see that the GND layer is on the bottom side.
This increases the distance from the signal trace, thus increases the stray inductance. On the other hand, placing the GND layer at a higher distance, allow decreasing the stray capacitance, which would have been higher if we would have trie to reduce the stray inductance. At high frequency, a bigger stray C would short the signal to the ground, limiting the achievable BW, thus we have to limit it.
Nevertheless, EMC is still an important topic, thus to limit the stray L, the OPA855 PCB layout offers a second ground layer next to the trace, directly on the top layer. The distance should be not smaller than the distance to the ground layer on the bottom, otherwise, the stray C will increase because of this second layer. The adjacent GND layer effectively reduces the stray L because of the vias placed next to the signal trace going from the top GND layer to the bottom one. This limits the current loop area by creating smaller stray L in parallel. Additionally, on the OPA855 PCB, once the signal traces are getting very close to the IC, the ground is removed to limit Cin.

DC-DC converters - GND under the inductor

The DC-DC converters use the inductor to store the energy in the form of a magnetic field. The energy is moved in and out during the different switching phases. In this article, we do not really care about how the DC-DC converters work, but we rather just keep in mind that the energy is stored within the inductor. The DC-DC converter efficiency is dependent on different factors, but one of these is how good we store the B field in the inductor itself. There are two major types of inductors, the shielded and not shielded ones. While today from EMC perspective designers are mostly using the shielded ones, the not shielded remains still cheaper, thus are widely used. Figure 2 shows a simplified picture of how the magnetic field may get outside the inductor by using the two different models (L1 is not shielded while L2 is shielded).

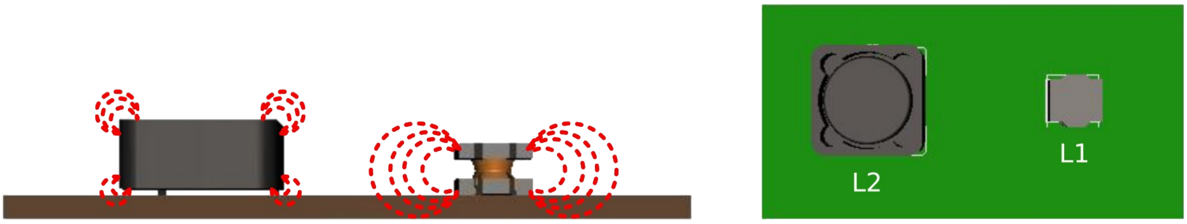

Figure 2: *Magnetic filed by shielded (L2) and not shielded (L1) inductors.*

It should be clear that the shielded inductor keeps the majority of the B field within the volume of interest, which is our inductor. The not shielded inductor has the B field going outside the inductor itself spreading energy away. This could be a problem from EMC perspective, but we will shortly see how the GND layer could create other challenges. Note that the not shielded inductor has often top and bottom ferrite heads, which help to keep the magnetic field close to the inductor, compared to the ones which are without heads. Now that we have seen the magnetic field going out, let's see what happens if we have a solid GND layer on the bottom layer. The Faraday Neumann Lenz equation, which is part of the known Maxwell's equations, tells us:

$$\oint_s \vec{E}\, ds = -\frac{d\Phi(\vec{B})}{dt}$$

This means that a variation of the B field flux generates an electric field. The Electric field exists in any circumstance, either we have a transformer, a ground layer, or simply air. Nevertheless, if the E field is located in an area where there is a metal, it can induce the free charges in it, to move, thus it will let a current flow on the metal. This current is known as Eddy's current. The – in the equation, tells us that the current flows in a way that it will generate a magnetic field that is opposite to the one that has generated the Eddy current, this derives from the energy conservation principle. Thus, if we have a GND layer under the inductor, the Eddy current will generate a B field that is opposite to the B field generated by the inductor. The result is that the total B field in the inductor gets reduced, decreasing the L itself. Indeed L is not only made by the wiring of the component itself, but strictly correlates to the B field flux that concatenates with the "component", so if we reduce the B field, also the concatenated flux will be reduced, reducing L itself.

So having the ground layer under the inductor will reduce our L and the efficiency of storing the energy with the B field. This also translates to reducing the efficiency of the DC-DC converter. If we take a simple filter made of an L and R, at the cut-off frequency, if we place a ground layer under the L, we can easily get a 0.5dB amplitude increase, which also means that we have increased the cutoff frequency of your filter. The Resonance frequency of the inductor may also change, but having it moved to the right is typically not a problem but rather a benefit.

Out of these considerations, it may not be beneficial having a GND layer under an inductor, nevertheless, very few changes can be seen if the inductor is shielded since the Eddy current will be generated only by the low B field that gets out from the inductor. From an EMC perspective having a solid ground is a preferred path in any case, since a slot on the ground may cause radiations. From what it has been said, you need to check the quality of your inductor. Eventually, as a trade-off, placing the GND layer not directly underneath the inductor, but rather on the bottom layer (by using 4 layers PCB) may already bring benefits. Also creating a GND net under the inductor could be a trade-off that may lead to reducing the Eddy current and have an advantage from the EMC perspective. By pushing the efficiency of your DC-DC converter you may try the GND slot under the inductor, but you should be neat in the EMC testing.

Conclusions

The article has shown the details of using the GND layer. As first thought, using it everywhere looks the good thing to do, but by looking at the details, there are areas where either removing or increase the distance between the GND layer and signal layer, could be actually beneficial. The article has studied different use cases, showing how it is important to place the GND layer in the right place to reduce either the stray inductance or capacitance. The article has also shown use cases where using the GND layer may actually create problems, such as for RF applications and DC-DC converters.

A single rule of "being good or bad" cannot be really extrapolated, nevertheless the idea of having a solid ground is good, but now we know that we have to think twice to avoid pitfalls and problems, especially from an EMC perspective.

About PCBWay

Bibliography

[1] www.LaurTec.it: official site where you can download the “EMC Testing” series.
[2] www.PCBWay.com: Service provider for PCB manufacturing, Assembly and 3D printing.

History

Date	Version	Author	Revision	Description
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